I/O Products

IC697VRM015

Fiber-Optic Reflective Memory with Interrupts

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Features

- High-speed, easy-to-use fiber-optic network (170 Mbaud serially)
- Data written to memory in one node is also written to memory in all nodes on the network
- Up to 2,000m between nodes and up to 256 nodes
- Data transferred at 6.2 Mbyte/s without redundant transfer
- Data transferred at 3.2 Mbyte/s with redundant transfer
- Any node on the network can generate an interrupt in any other node on the network or in all network nodes with a single command
- Error detection
- Redundant transmission mode for suppressing errors
- No processor overhead
- No processor involvement in the operation of the network
- 256 Kbyte of Reflective Memory (SRAM)
- A24:A32:D32:D16:D8 memory access
- Single 6U VMEbus board

Product Overview

The IC697VRM015 is a high-performance, multidrop VME-to-VME network. Data is transferred by writing to on-board global RAM. The data is automatically sent to the same location in memory on all Reflective Memory boards on the network.

The Reflective Memory concept provides a fast and efficient way of sharing data across distributed computer systems. Reflective Memory allows data to be shared between up to 256 independent systems (nodes) at rates up to 6.2 Mbyte/s. Each Reflective Memory board is configured with 256 Kbyte of on-board SRAM.



The local SRAM provides fast Read access times to stored data. Writes are stored in local SRAM and broadcast over a high-speed fiber-optic data path to other Reflective Memory nodes. The transfer of data between nodes is software transparent, so no I/O overhead is required. Transmit and Receive FIFOs buffer data during peak data rates to optimize CPU and bus performance to maintain high data throughput.

Reflective Memory also allows interrupts to one or more nodes by writing to a byte register. These interrupt (three level, user definable) signals may be used to synchronize a system process, or used to follow any data that may have preceded it. The interrupt always follows the data to ensure the reception of the data before the interrupt is acknowledged.

Reflective Memory requires no initialization unless interrupts are being used. If interrupts are used, vectors and interrupt levels must be written to on-board registers to arm the interrupts.

Each node on the system has a unique identification number between 0 and 255. The node number is established during hardware system integration by placement of jumpers on the board. This node number can be read by software by accessing an on-board register. In some applications, this node number would be useful in establishing the function of the node.

Link Arbitration

The Reflective Memory system is a fiber-optic daisy chain ring. Each transfer is passed from node to node until it has gone all the way around the ring and reaches the originating node. Each node retransmits all transfers that it receives except those that it had originated. Nodes are allowed to insert transfers between transfers passing through.

Interrupt Transfers

In addition to transferring data between nodes, the Reflective Memory board will allow any processor in any node to generate an interrupt on any other node. These interrupts would generally be used to indicate to the receiving node that new data has been sent and is ready for processing. These interrupts are also used to indicate that processing of old data is completed and the receiving node is ready for new data.

Three interrupts are available. The user may define the function, priority, and vector for each interrupt. Any processor can generate an interrupt on any other node on the network. In addition, any processor on the network can generate an interrupt on all nodes on the network. Interrupts are generated by simply writing to a single Reflective Memory register.

All data and interrupt command transfers contain the node number of the node that originated the transfer. This information is used primarily so the originating node can remove the transfer from the network after the transfer has traversed the ring. The node identification is also used by nodes receiving interrupt commands. When a node receives an interrupt command for itself, it places the identification number of the originating node in a FIFO. Up to 512 interrupts can be stacked in the FIFO. During the interrupt service routine, the identification of the interrupting node can be read from the FIFO.

Error Management

Errors are detected by the Reflective Memory with the use of the error detection facilities of the TAXI chipset and additional parity encoding and checking. The error rate of the Reflective Memory board is a function of the rate of errors produced in the optical portion of the system. This optical error rate depends on the length and type of fiber-optic cable.

Assuming an optical error rate of 10^{-12}, the error rate of the Reflective Memory is 10^{-10} transfers/transfer. However, the rate of undetectable errors is less than 10^{-20} transfers/transfer. When a node detects an error, the erroneous transfer is removed from the system and a VMEbus interrupt is generated, if armed.

Reflective Memory can be operated in a redundant transfer mode in which each transfer is transmitted twice. In this mode of operation, the first of the two transfers is used unless an error is detected in which case the second transfer is used. In the event that an error is detected in both transfers, the node removes the transfer from the system. The probability of both transfers containing an error is 10^{-20}, or about one error every 372,000 years at maximum data rate.

Protection Against Lost Data

Data received by the node from the fiber-optic cable is error checked and placed in a receive FIFO. Arbitration with accesses from the VMEbus then takes place and the data is written to the node's SRAM and to the node's transmit FIFO. Data written to the board from the VMEbus is placed directly into SRAM and into the transmit FIFO. Data in the transmit FIFO is transmitted by the node over the fiber-optic cable to the next node. Data could be lost if either FIFO were allowed to become full.

The product is designed to prevent either FIFO becoming full and overflowing. It is important to note the only way that data can start to accumulate in FIFOs is for data to enter the node at a rate greater than 6.2 or 3.2 Mbyte/s in redundant mode. Since data can enter from the fiber and from the VMEbus, it is possible to exceed these rates. If the transmit FIFO becomes half-full, a bit in the Status Register is set and, if armed, an interrupt is generated. This condition is an indication that writes to the Reflective Memory should be suspended until the FIFO becomes less than half-full. If the half-full indication is ignored and the transmit FIFO becomes full, then writes to the Reflective Memory will be acknowledged with a bus error. With VMEbus writes being blocked by the bus error, data cannot overflow in the receive FIFO.

Network Monitor

There is a bit in a Status Register that can be used to verify that data is traversing the ring (that is, the ring is not broken). This can also be used to measure network latency.

Specifications

Memory Size: 256 Kbyte

Memory: Addressable on 256 Kbyte boundaries

Access Time:
400ns (worst-case arbitration)

200ns (best-case arbitration)

Transfer Rate:
6.2 Mbyte/s (longword accesses) without redundant transfer

3.2 Mbyte/s (longword accesses) with redundant transfer

VMEbus: This product complies with the VMEbus specification (ANSI/IEEE STD 1014-1987, IEC 821 and 297), with the following mnemonics: A32: A24: D32/D16/D08 (EO): Slave: 39/3D:09/0D
Form factor: 6U

Cable Requirements: ST Type Fiber-Optic cables Multimode; 62.5 Micron core

Transmitters operate at 1,300nm at 170 Mbaud

Cable Length: 2,000m maximum between nodes

Configuration: Daisy chain ring up to 256 nodes

Temperature Range: 0 to 55°C, operating

-40 to 85°C, storage

Relative Humidity: 20 to 80%, noncondensing

Power Requirements: 5.0A maximum at +5VDC

MTBF: 142,400 hours (MIL STD 217F)

Data Transfers

Data written into the Reflective Memory is broadcast to all nodes on the network without further involvement of the sending or receiving nodes. Data is transferred from memory locations on the sending nodes to corresponding memory locations on the receiving nodes.

A functional block diagram of the Reflective Memory is shown in Figure 1.

Agency Approvals: UL1604 with C-UL

Certification by Underwriters Laboratory for use in Class 1, Div. 2, Groups A, B, C, D Hazardous Locations. Board complies with applicable CSA Standards as evaluated by UL. The C-UL mark is accepted throughout Canada.

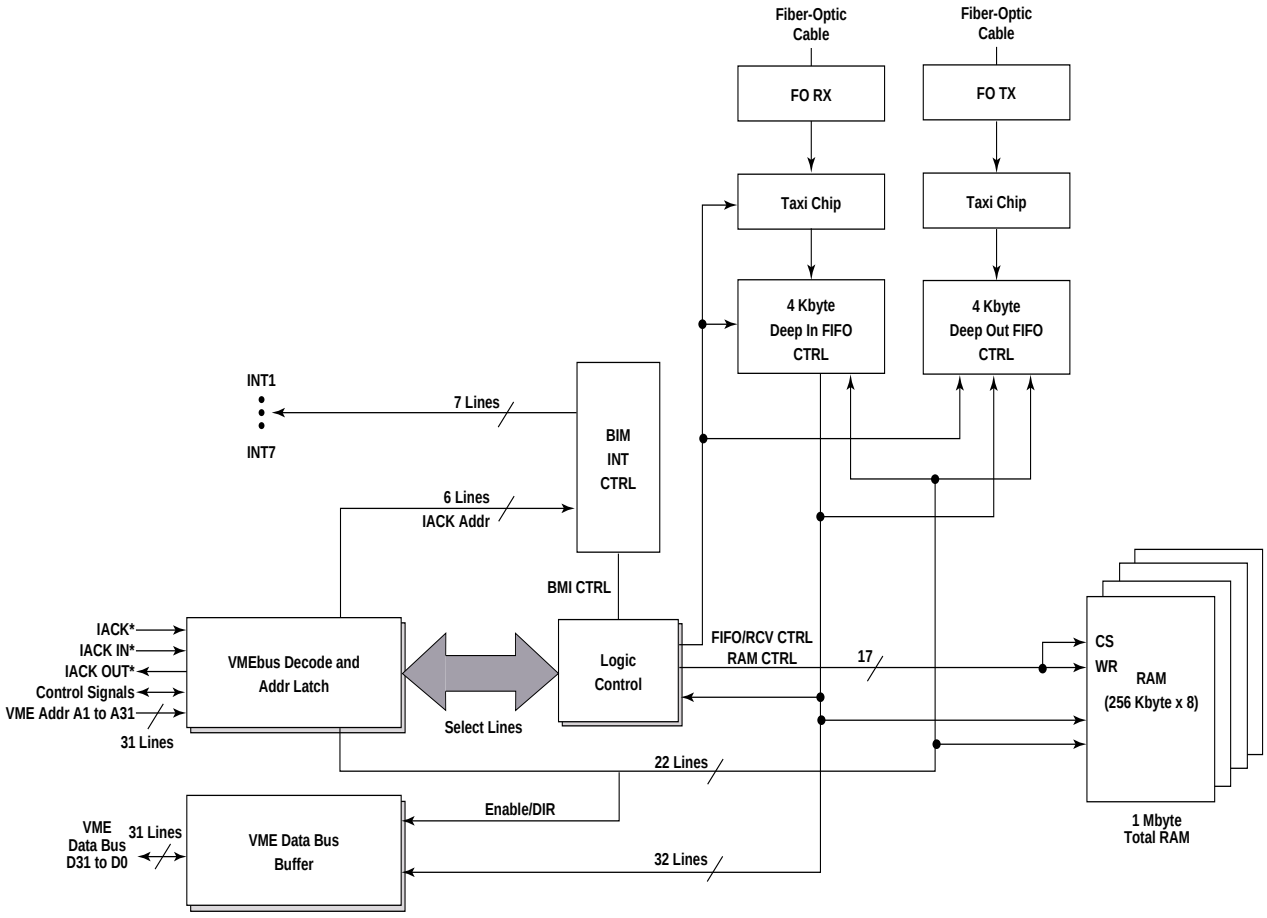


Figure 1. Reflective Memory Block Diagram